CEP5815

PWM Power Switch Fixed 65KHz Fsw

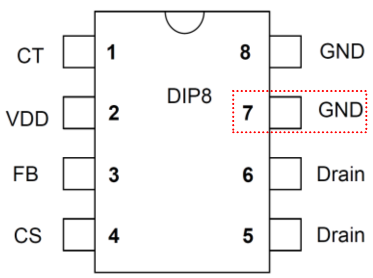
■ FEATURES

- ➢ Less than 75mW Standby Power
- ➢ Built-in 600V Power MOSFET
- ➢ Programmable OLP Debounce Time
- ➢ Proprietary η-Balance Control to Boost Light Load Efficiency
- ➢ Proprietary “Zero OCP/OPP Recovery Gap” Control
- ➢ Fixed 65KHz Switching Frequency
- ➢ Built-in Soft Start Function
- ➢ Very Low Startup Current
- ➢ Current Mode Control
- ➢ Frequency Reduction and Burst Mode Control for Energy Saving
- ➢ Built-in Frequency Shuffling
- ➢ Built-in Synchronous Slope Compensation
- ➢ Cycle-by-Cycle Current Limiting
- ➢ Built-in Leading Edge Blanking (LEB)
- ➢ Constant Power Limiting
- ➢ Pins Floating Protection
- ➢ Audio Noise Free Operation
- ➢ VDD OVP & Clamp
- ➢ VDD Under Voltage Lockout (UVLO)

■ APPLICATIONS (Offline AC/DC Fly-back Converter for)

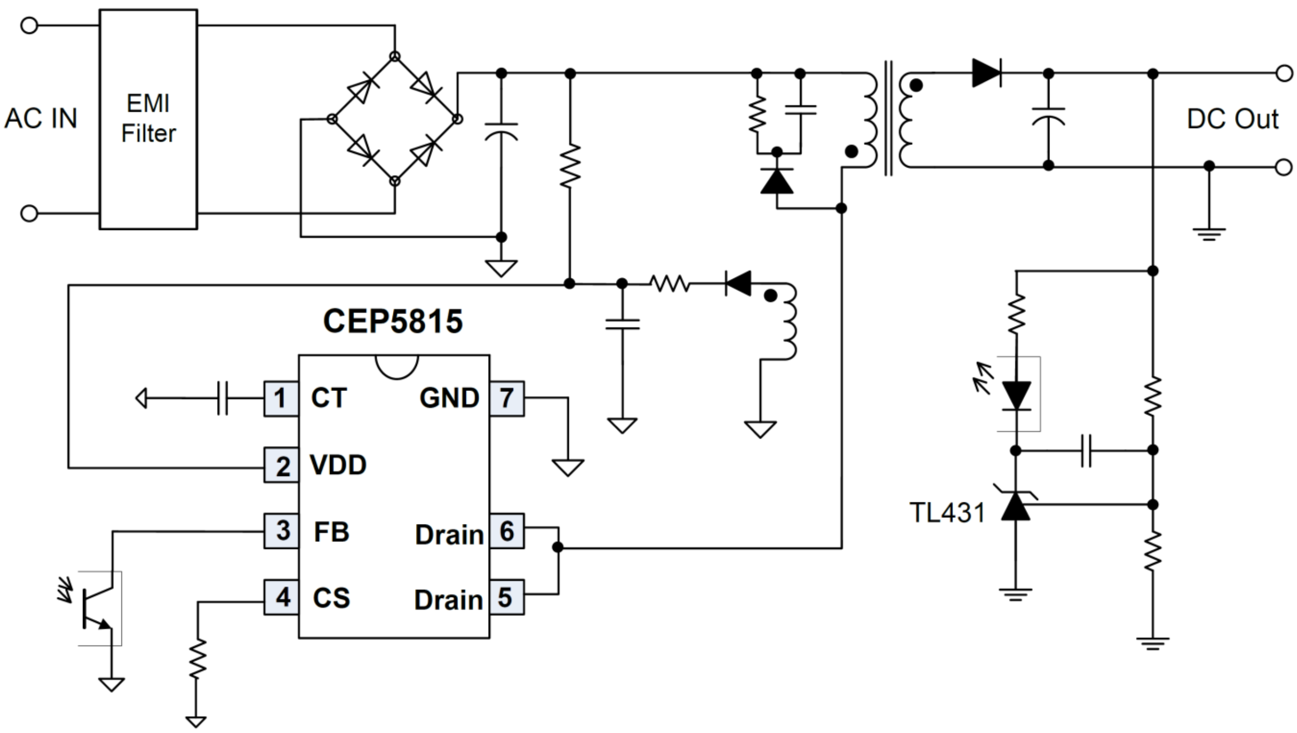
- ➢ AC/DC Adaptors
- ➢ Open-frame SMPS

■ PACKAGE and SIMPLIFIED APPLICATION DIAGRAM



Note:
1, CEP5815DP8 is DIP8.
2, CEP5815DP7 is DIP7.
(The PIN-7 is delete.)

Pin No.	Pin Name	I/O	Description
1	CT	I	Pin for program OLP debounce time. If this pin is floating, the OLP time is 55ms. If an external capacitor is connected between CT and GND, the OLP debounce time can be programmable.
2	VDD	P	IC power supply pin.
3	FB	I	Voltage feedback pin. The loop regulation is achieved by connecting a photo-coupler to this pin. PWM duty cycle is determined by this pin voltage and the current sense signal at Pin 4.
4	CS	I	Current sense input pin.
5-6	Drain	P	High voltage power MOSFET drain connection.
7-8	GND	P	Ground. For CEP5815DP, pin 7 and pin 8 are Ground.



GENERAL DESCRIPTION

CEP5815 is a high performance, high efficiency, highly integrated current mode PWM power switch for offline fly-back converter applications.

In CEP5815, PWM switching frequency with shuffling is fixed to 65KHz and is trimmed to tight range. When the output power demands decrease, the IC decreases switching frequency based on the Proprietary η-Balance control to boost power conversion efficiency at the light load. When output power falls below a given value, the IC enters into burst mode and provides excellent efficiency without audio noise.

The IC can achieve “Zero OCP/OPP Recovery Gap” using ChipExtra’s proprietary control algorithm. Meanwhile, the OCP/OPP variation versus universal line input is compensated.

The IC has built-in synchronized slope compensation to prevent sub- harmonic oscillation at high PWM duty output. The IC also has built-in soft start function to soften the stress on the MOSFET during power on period.

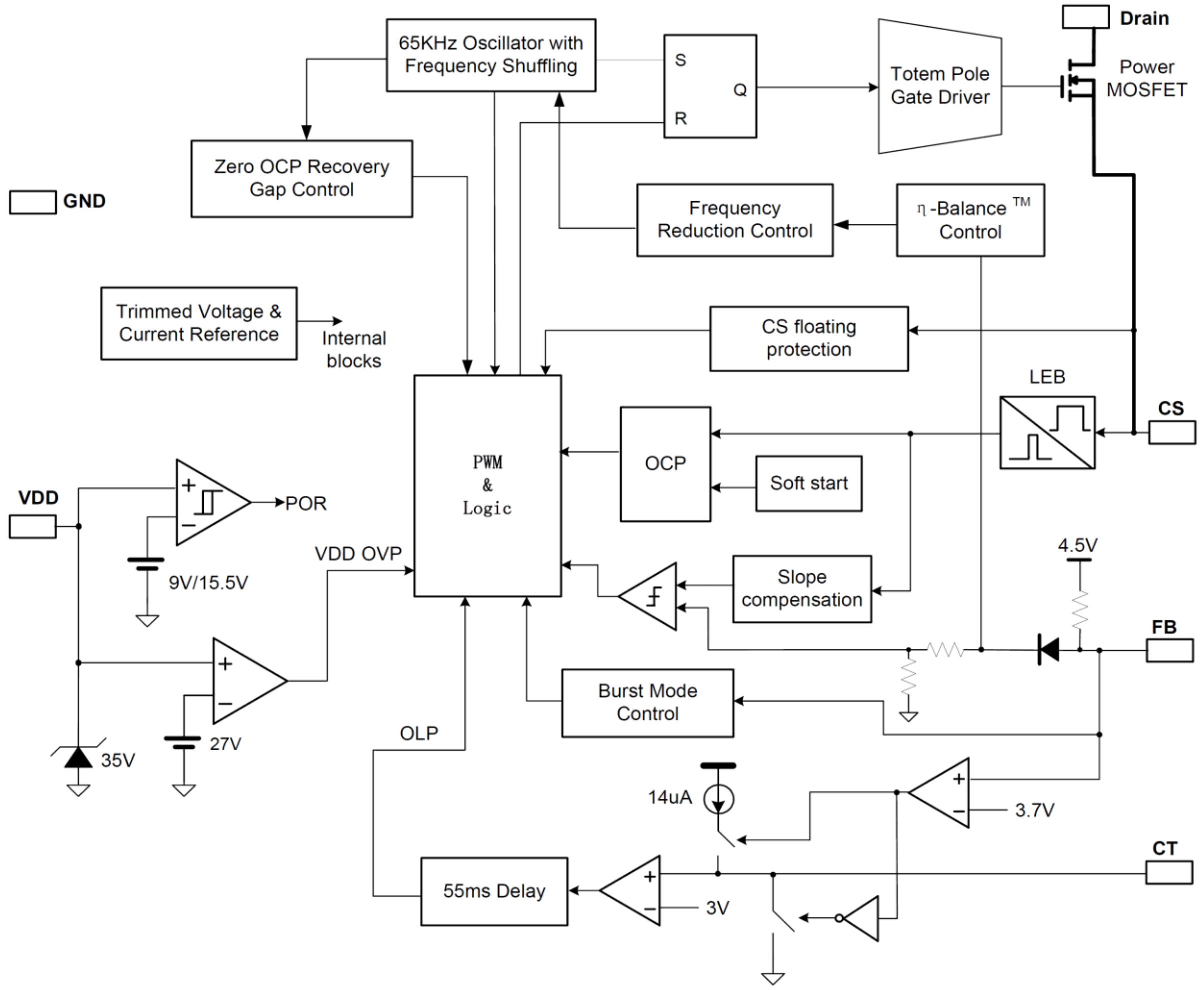
CEP5815 integrates functions and protections of Under Voltage Lockout (UVLO), VCC Over Voltage Protection (OVP), Cycle-by-cycle Current Limiting (OCP), Pins Floating Protection, Over Load Protection (OLP), VCC Clamping, Leading Edge Blanking (LEB), etc.

CEP5815 is available in DIP8 and DIP7 packages.

Ordering Information

Part Number	Top Mark	Package	Tape & Reel
CEP5815DP7	C5815 YYWW XX	DIP7	YES
CEP5815DP8		DIP8	

Block Diagram



■ **Output Power Table(**Note 1**)**

Part Number	230VAC ± 15% (Note 2)		85-265VAC	
	Adapter(Note 3)	Open Frame(Note 4)	Adapter	Open Frame
CEP5815	18W	26W	15W	18W

■ **Absolute Maximum Ratings** (Note 5)

Parameter	Value	Unit
VDD DC Supply Voltage	35	V
VCC DC Clamp Current	10	mA
Drain pin	-0.3 to 600	V
FB, CS voltage range	-0.3 to 7	V
Package Thermal Resistance (DIP-8)	84	℃/W
Package Thermal Resistance (DIP-7)	88	℃/W
Maximum Junction Temperature	150	℃
Operating Temperature Range	-40 to 85	℃
Storage Temperature Range	-65 to 150	℃
Lead Temperature (Soldering, 10sec.)	260	℃
ESD Capability, HBM (Human Body Model)	3	kV
ESD Capability, MM (Machine Model)	250	V

■ **Recommended Operation Conditions** (Note 6)

Parameter	Value	Unit
Supply Voltage, VDD	11 to 25	V
Operating Ambient Temperature	-40 to 85	℃

Note 1. The Max. output power is limited by junction temperature
Note 2. 230VAC or 100/115VAC with doublers
Note 3. Typical continuous power in a non-ventilated enclosed adapter with sufficient drain pattern as a heat sink at 50 ℃ ambient.
Note 4. Max. practical continuous power in a open-frame design with sufficient drain pattern as a heat sink at 50 ℃ ambient.
Note 5. Stresses beyond those listed under **"**Absolute Maximum Ratings**"** may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
Note 6. The device is not guaranteed to function outside its operating conditions.

■ ELECTRICAL CHARACTERISTICS

(TA = 25℃, VDD=18V, if not otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Supply Voltage Section (VDD Pin)						
UVLO(ON)	VDD Under Voltage Lockout Exit (Startup)		14.5	15.5	16.5	V
UVLO(OFF)	VDD Under Voltage Lockout Enter		8	9	9.8	V
I_Startup	VDD Start up Current	VDD =UVLO(ON)-1V, Measure current into VDD		3	15	uA
I_VDD_Op	Operation Current	VFB=3V		2.0	3.5	mA
VDD_OVP	VDD Over Voltage Protection trigger		25	27	29	V
VDD_Clamp	VDD Zener Clamp Voltage	I(VDD) = 10mA		35.5		V
T_Softstart	Soft Start Time			4		mSec
Feedback Input Section(FB Pin)						
VFB_Open	FB Open Voltage			4.5		V
IFB_Short	FB short circuit current	Short FB pin to GND, measure current	0.22	0.33	0.45	mA
AVCS	PWM Input Gain	ΔVFB /ΔVcs		1.6		V/V
VFB_min_duty	FB under voltage gate clock is off.			1.0		V
VTH_PL	Power Limiting FB Threshold Voltage			3.7		V
TD_PL_min	Minimum Power limiting Debounce Time	CT is floating		43		mSec
ZFB_IN	Input Impedance			14		Kohm
Current Sense Input Section (CS Pin)						
Vth_OC_min	Internal current limiting threshold	Zero duty cycle	0.70	0.75	0.80	V
T_blanking	CS Input Leading Edge Blanking Time			250		nSec
TD_OC	Over Current Detection and Control Delay			90		nSec
Oscillator Section						
FOSC	Normal Oscillation Frequency		60	65	70	KHZ
ΔF(shuffle)/Fosc	Frequency shuffling range	Note 7	-4		4	%
Δf_Temp	Frequency Temperature Stability	-20oC to 100 ℃ (Note 8)		5		%
Δf_VDD	Frequency Voltage Stability	VDD = 12-25V,		5		%
Duty_max	Maximum Duty cycle		75	80	85	%
F_BM	Burst Mode Base Frequency			22		KHZ
OLP Debounce Program Section (CT Pin)						
I_CT	Output Current of CT Pin		10	14	18	uA
VTH_CT	Comparator threshold for OLP debounce time			3		V
Power MOSFET Section						
BVdss	Power MOSFET Drain Source Breakdown Voltage		600			V
Rdson	Static Drain -Source On Resistance	I(Drain)=1A		3.8	4.7	Ω
Idss	Zero Gate Voltage Drain Current				1	uA
Td(on)	Turn-on delay time			9		ns
Td(off)	Turn-off delay time			24		ns

Note 7. These parameters, although guaranteed, are not 100% tested in production
Note 8. Guaranteed by design.

■ OPERATION DESCRIPTION

CEP5815 is a high performance, high efficiency, highly integrated current mode PWM power switch for offline fly-back converter applications. The built-in advanced energy saving with high level protection features improves the SMPS reliability and performance without increasing the system cost.

■ UVLO and Startup Operation

Fig.1 shows a typical startup circuit. Before the IC begins switching operation, it consumes only startup current (typically 3uA) and current supplied through the startup resistor Rst charges the VDD hold-up capacitor Cdd. When VDD reaches UVLO turn-on voltage of 15.5V (typical), CEP5815 begins switching and the IC current consumed increased to 2mA (typical). The hold-up capacitor Cdd continues to supply VDD before the energy can be delivered from auxiliary winding Na. During this process, VDD must not drop below UVLO turn-off voltage (typical 9V). The selection of Rst and Cdd should be a trade off between the power loss and startup time.

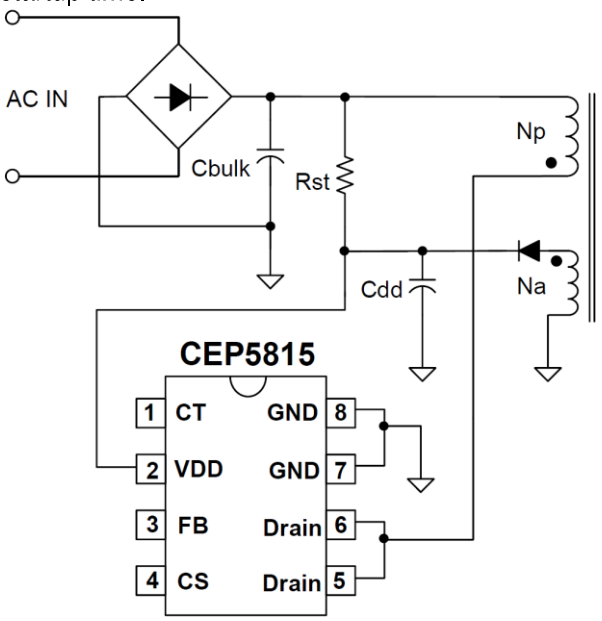


Fig.1

■ Low Operating Current

The operating current in CEP5815 is as small as 2mA (typical). The small operating current results in higher efficiency and reduces the VDD hold-up capacitance requirement.

■ Soft Start

CEP5815 features an internal 4ms (typical) soft start that slowly increases the threshold of cycle-by-cycle current limiting comparator during startup sequence. It helps to prevent transformer saturation and reduce the stress on the secondary diode during startup. Every restart attempt is followed by a soft start activation.

■ "Zero OCP/OPP Recovery Gap" Control

The definition of OCP or OPP recovery gap of a power adaptor is illustrated in Fig.2. At T0, assuming an adaptor is at full loading mode. If the loading keeps increasing, then the system will output maximum power P_opp, which will trigger OPP protection at the same time. After the OPP protection is triggered, usually the system will enter into the auto-recovery mode, in burst manner. If the system power demand decreases below P_recovery, then system will enter into normal mode again, as shown in Fig.2. The difference between P_opp and P_recovery is defined as "OPP Recovery Gap", which can cause system startup failure especially in 90VAC full load startup.

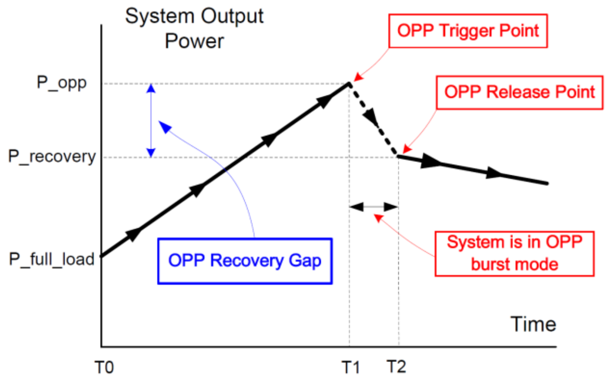


Fig.2

CEP5815 can achieve "Zero OCP/OPP Recovery Gap" in the whole universal AC input range using SiFirst's proprietary control algorithm.

■ Oscillator with Frequency Shuffling

PWM switching frequency in CEP5815 is fixed to 65KHz and is trimmed to tight range. To improve system EMI performance, CEP5815 operates the system with ±4% frequency shuffling around setting frequency.

■ Synchronous Slope Compensation

In CEP5815, the synchronous slope compensation circuit is integrated by adding voltage ramp onto the current sense input voltage for PWM generation.

This greatly improves the close loop stability at CCM and prevents the sub-harmonic oscillation and thus reduces the output ripple voltage.

■ Programmable OLP Debounce Time

Connecting a capacitor CCT from CT pin to GND according to the equation below to program the OLP debounce time. In OLP debounce time, an internal current (14uA, typical) charges CCT, when CT pin voltage reaches 3V, an internal 43ms debounce is triggered. When internal 43ms debounce time is over, the OLP protection is triggered and the system will enter into auto recovery protection mode.

$$T_{OLP\_debounce} = \frac{3V * C_{CT}}{14uA} + 43ms$$

If CT pin is floating, the OLP debounce time is 43ms. Otherwise, the OLP debounce time can be programmed by CT capacitor.

■ **Proprietary η-Balance Control**

The efficiency requirement of power conversion is becoming tighter than before. These new energy standards focus on the average efficiency of the whole loading range. Therefore, the light load efficiency is becoming more and more important.

In CEP5815, a proprietary η-Balance control is integrated to boost the light load efficiency. As shown in Fig.3, when the loading becomes light, the IC will reduce the PWM switching frequency according to an optimized frequency reduction curve. The specific frequency reduction curve and the power at a frequency are determined by the output of η-Balance control. For example, P1 is at full load, P2 is at 75% full load, P3 and P4 are 50% and 25% full load respectively. The η - Balance control can provide higher average efficiency than conventional frequency reduction technique, as illustrated in Fig.3

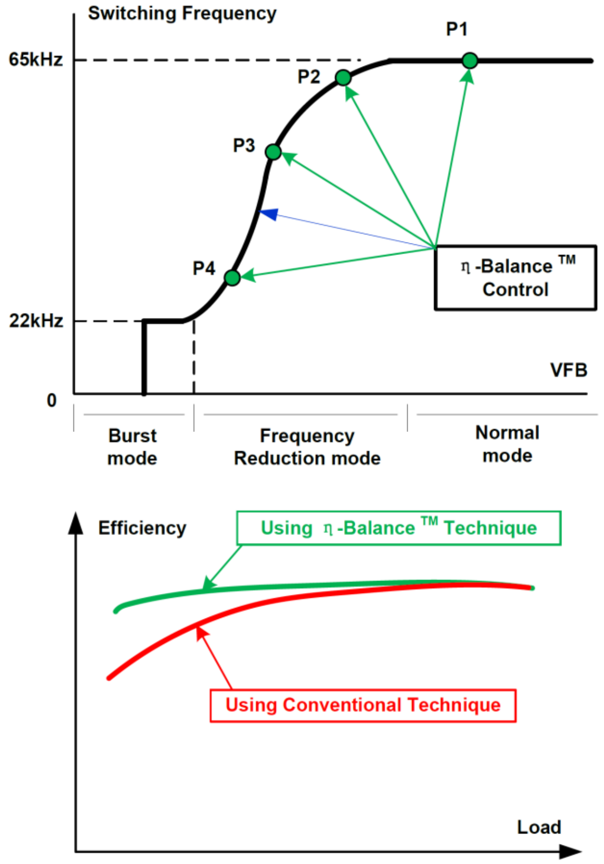


Fig.3

■ **Leading Edge Blanking (LEB)**

Each time the power MOSFET is switched on, a turn-on spike occurs across the sensing resistor. The spike is caused by primary side capacitance and secondary side rectifier reverse recovery. To avoid premature termination of the switching pulse, an internal leading edge blanking circuit is built in. During this blanking period (250ns, typical), the PWM comparator is disabled and cannot switch off the gate driver. Thus, external RC filter with a small time constant is enough for current sensing.

■ **Burst Mode Control**

When the loading is very small, the system enters into burst mode. When VFB drops below Vskip, CEP5815 will stop switching and output voltage starts to drop, which causes the VFB to rise. Once VFB rises above Vskip, switching resumes. Burst mode control alternately enables and disables switching, thereby reducing switching loss in standby mode.

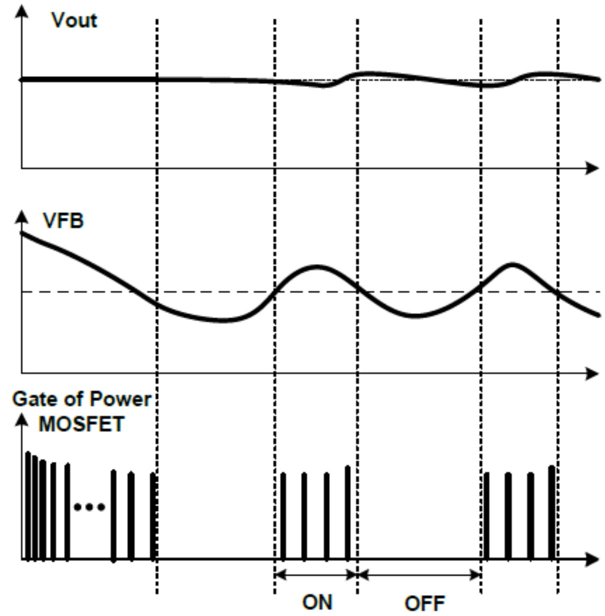


Fig.4

■ **Auto Recovery Mode Protection**

As shown in Fig.5, once a fault condition is detected, switching will stop. This will cause VDD to fall because no power is delivered form the auxiliary winding. When VDD falls to UVLO (off) (typical 9V), the protection is reset and the operating current reduces to the startup current, which causes VDD to rise, as shown in Fig.4. However, if the fault still exists, the system will experience the above mentioned process. If the fault has gone, the system resumes normal operation. In this manner, the auto restart can alternatively enable and disable the switching until the fault condition is disappeared.

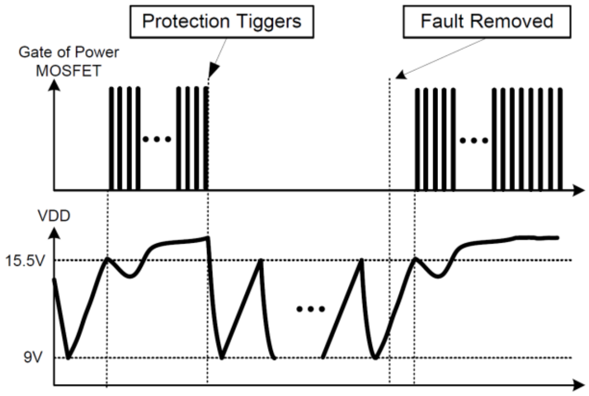


Fig.5

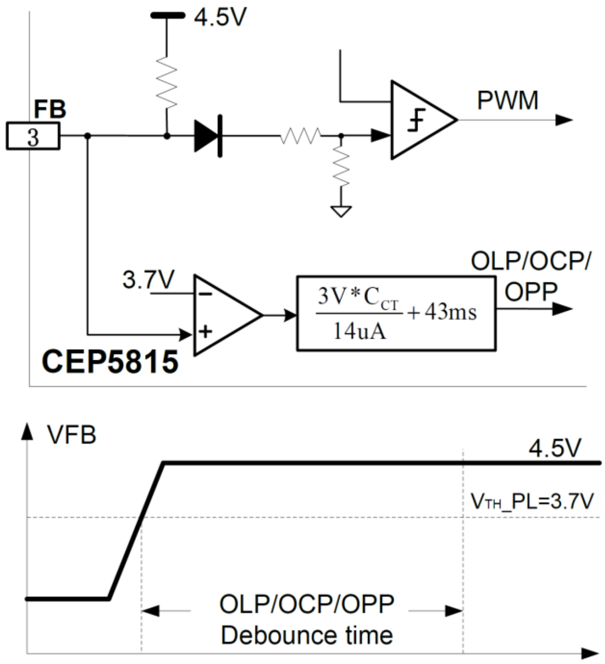


Fig.6

- **VDD OVP(Over Voltage Protection)**

VDD OVP (Over Voltage Protection) is implemented in CEP5815 and it is a protection of auto-recovery mode.

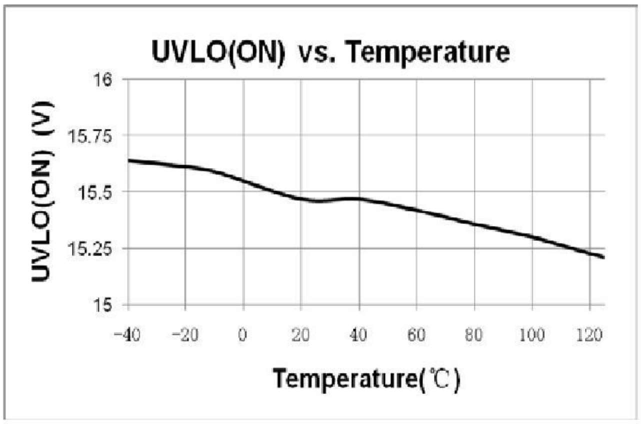
- **Over Load Protection (OLP) / Over Current Protection (OCP) / Over Power Protection (OPP) / Open Loop Protection (OLP)**

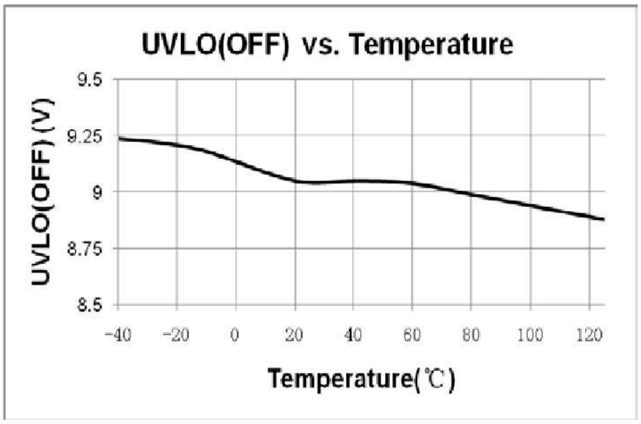
When OLP/OCP/OPP/Open Loop occurs, a fault is detected. If this fault is present for more than TOLP_debounce , the protection will be triggered, the IC will experience an auto-recovery mode protection as mentioned above, as shown in Fig.6. The TOLP_debounce debounce time is to prevent the false trigger from the power-on and turn-off transient.

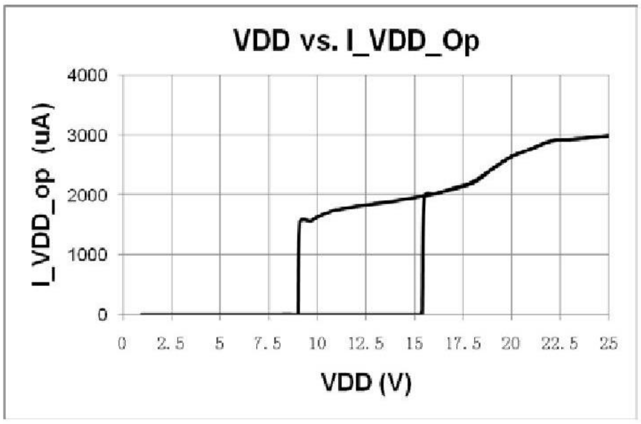
- **Soft Gate Drive**

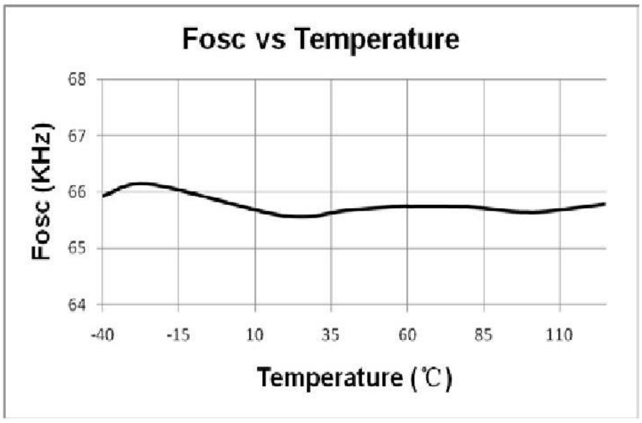
The driving stage of CEP5815 is a soft totem-pole gate driver to minimize EMI. Cross conduction has been avoided to minimize heat dissipation, increase efficiency, and enhance reliability.

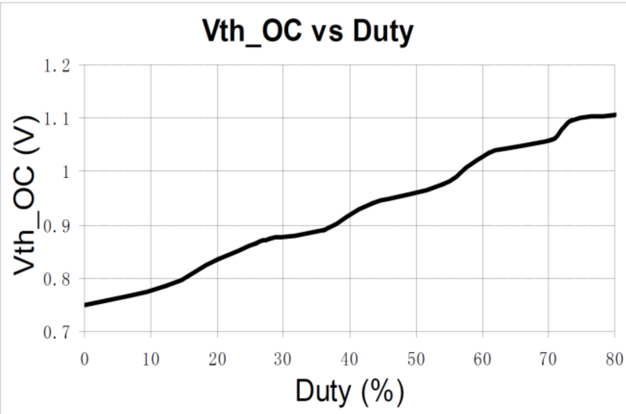
■ CHARACTERIZATION PLOTS

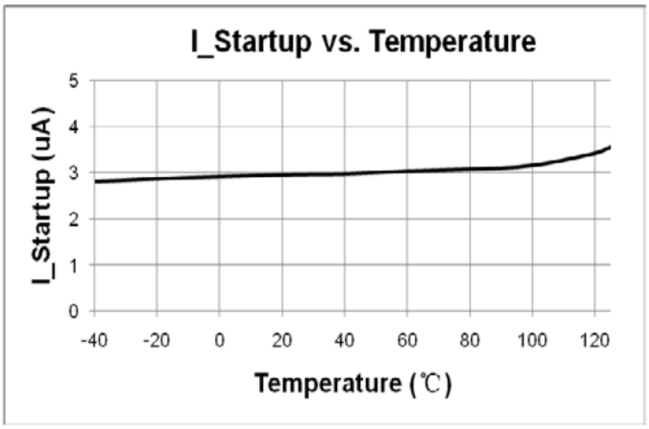


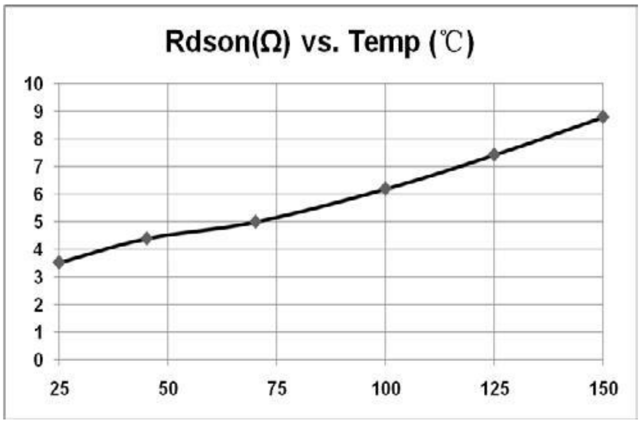




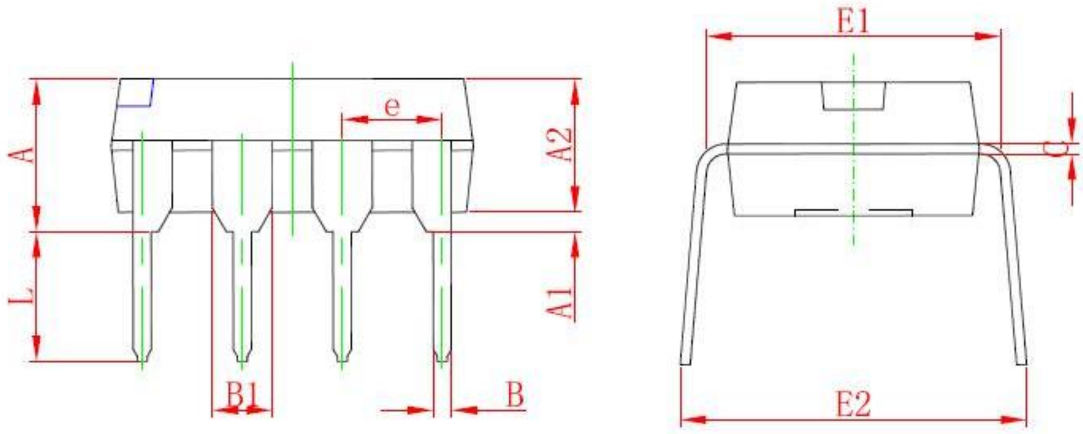


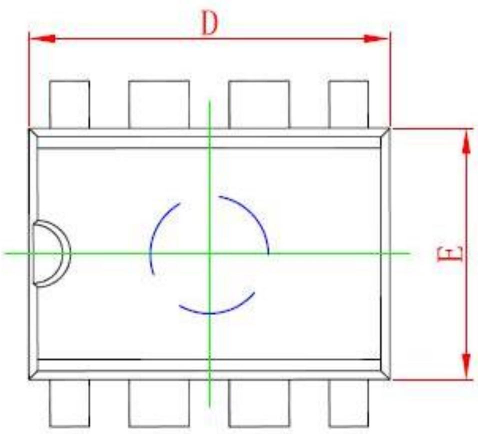






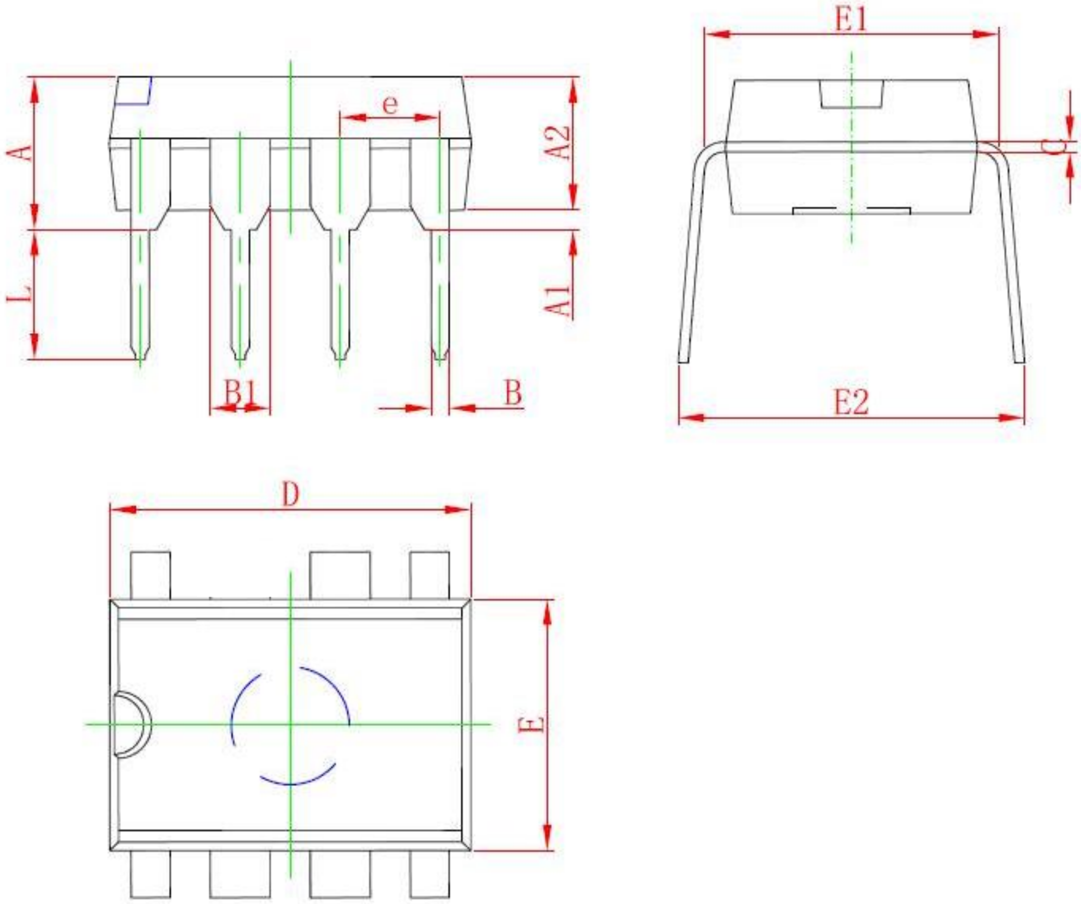
■ **PACKAGE OUTLINE(DIP-8)**





Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	3.710	5.334	0.146	0.210
A1	0.381		0.015	
A2	3.175	3.600	0.125	0.142
B	0.350	0.650	0.014	0.026
B1	1.524 (BSC)		0.06 (BSC)	
C	0.200	0.360	0.008	0.014
D	9.000	10.160	0.354	0.400
E	6.200	6.600	0.244	0.260
E1	7.320	7.920	0.288	0.312
e	2.540 (BSC)		0.1 (BSC)	
L	2.921	3.810	0.115	0.150
E2	8.200	9.525	0.323	0.375

■ **PACKAGE OUTLINE(DIP-7)**



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B1	1.524 (BSC)		0.06 (BSC)	
C	0.200	0.360	0.008	0.014
D	9.000	10.160	0.354	0.400
E	6.200	6.600	0.244	0.260
E1	7.320	7.920	0.288	0.312
e	2.540 (BSC)		0.1 (BSC)	
L	2.921	3.810	0.115	0.150
E2	8.200	9.525	0.323	0.375